Thermocouple conditioner draws μA

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This complete digital output, thermocouple signal conditioner (**Fig 1a**) produces a 0- to 1-kHz output in response to sensing a 0 to 100°C temperature excursion. The circuit includes cold-junction compensation, and accuracy is within 1°C with stable 0.1°C resolution. Additionally, the circuit operates from a single supply that can range from 4.75 to 10V. The circuit consumes a maximum of 360 μA.

The LT1025 provides an appropriately scaled cold-junction compensation voltage to the type K thermocouple. As a result, the voltage at point A in **Fig 1a** varies from 0 to 4.06 mV over a sensed 0 to 100°C range (type K thermocouples have a slope of 40.6 μV/°C). The remaining components form a voltage-to-frequency converter that directly converts this mV level signal without the usual dc gain stage. The thermocouple biases the negative input of IC_1, a chopper-stabilized op amp. IC_1's output drives a crude V/F converter, comprised of Q_2, a series of 74C14 inverters,

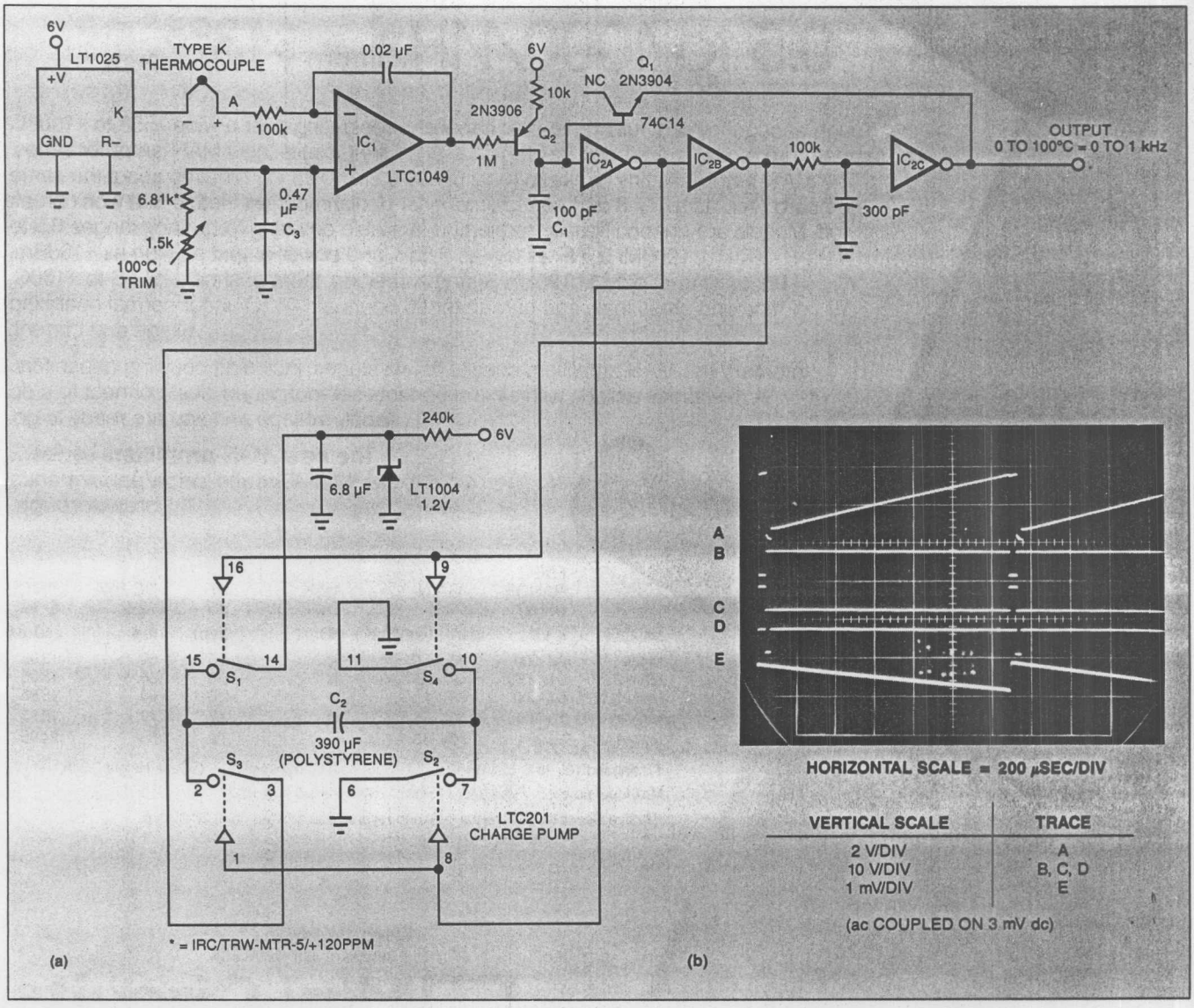

***Fig 1—This temperature-to-frequency converter (a) outputs** a signal with frequencies ranging from 0 to 1 kHz in response to temperatures between 0 and 100°C. The waveforms in **b** illustrate the circuit's operations at various points.*

and other associate components. Each V/F output pulse dispenses a fixed quantity of charge into C_3 from C_2 via the LTC201-based charge pump. C_3 integrates the charge packets, producing a voltage at IC_1's positive input. IC_1's output forces the V/F converter to run at whatever frequency is required to balance the amplifier's inputs. This feedback action eliminates error terms caused by drift and nonlinearities in the V/F converter. The output frequency is solely a function of the dc conditions at IC_1's inputs. The 0.02-μF capacitor forms a dominant response pole at IC_1, which stabilizes the loop.

Fig 1b demonstrates the circuit's operation. IC_1's output biases current source Q_2 producing a ramp (Trace A) across C_1. When the ramp crosses IC_{2A}'s threshold, the cascaded inverter chain switches, producing complementary outputs at IC_{2A} (Trace B) and IC_{2B} (Trace C). IC_{2C}'s RC delayed response (Trace D) turns on diode-connected Q_1, thereby discharging C_1 and resetting the ramp. The ramp aberrations that occur just before the reset in Trace A are due to transient input current from IC_{2A} during switching (near top of ramp). Q_1's V_{BE} diode rounding and reverse-charge transfer (bottom of ramp) account for the discontinuities during the ramp's low point.

The complementary inverter outputs from IC_{2A} and IC_{2B} clock the LTC201 switched-based charge pump. S_1 and S_4 alternately charge C_2 to the LT1004's reference voltage. C_2 discharges into C_3 through S_2 and S_3. Each time this cycle occurs, C_3's voltage is forced up (Trace E). C_3's average voltage is set by the 6.81k and 1.5k resistors in parallel with it. IC_1 servo controls the repetition rate of the V/F converter to bring its inputs to the same value, closing the control loop.

To calibrate this circuit, disconnect the thermocouple and drive point A with 4.06 mV. Next, set the 1.5k potentiometer for exactly a 1-kHz output. Connect the thermocouple, and the circuit is ready for use. If you have to replace the thermocouple, recalibration isn't necessary. Also note that this circuit can directly digitize any mV-level signal by deleting the LT1025/thermocouple pair and directly driving point A.

(EDN BBS /DI_SIG #960) EDN

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Scope's beam locates missing codes

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Fig 1's circuit allows you to detect an A/D converter's missing codes at a glance because all the codes appear on an oscilloscope CRT as dots in a matrix. The scope will display rows of dots each of which represents a valid code. When a code is missing, the scope's X/Y trajectory either completely skips over that position or remains settled on that point for too short a time to produce a visible spot. The circuit in **Fig 1** specifically tests any 6-bit flash ADC equivalent to the standard CA3300 such as the MP7682 from Micro Power Systems (Santa Clara, CA) or the CA3306 from Harris Semiconductor (Melbourne, FL). For a 6-bit flash ADC, the matrix has 8 pixels/side, and the process takes a few seconds. You can extend this idea to test 8-bit and higher-resolution converters.

In **Fig 1**, IC_1 is the ADC under test. It converts a sawtooth input signal that spans the entire thermometric range. The 6-bit output drives a fast DAC whose output voltage connects to the Y channel of a scope operating in XY mode. The three LSBs of the ADC's output also drive a second DAC, the output of which connects to the scope's X channel. Both DACs work from the opposite clock edge of the ADC to ensure that conversion is complete and that the data is stable. The DAC output includes some dc bias.

Operating from an LM136 5V reference, one LF355 JFET-input op amp supplies the reference voltage to the DACs and helps cancel the bias voltages of the DACs by serving as one of the EL2020 op-amp inputs. Another LF355 provides the ADC's reference. The two EL2020 fast, transimpedance op amps subtract the bias voltage from the DAC outputs and send the two results to the corresponding channels of the scope.

As **Fig 1** indicates, the scope displays the codes as a square matrix of $2^{(N/2)}$ dots/side when N is even. During the ramp input's rise times, the matrix fills repeatedly with dots in a left-to-right and bottom-to-top sequence. **Fig 1** also details the events that take place during the settlement transient. The state